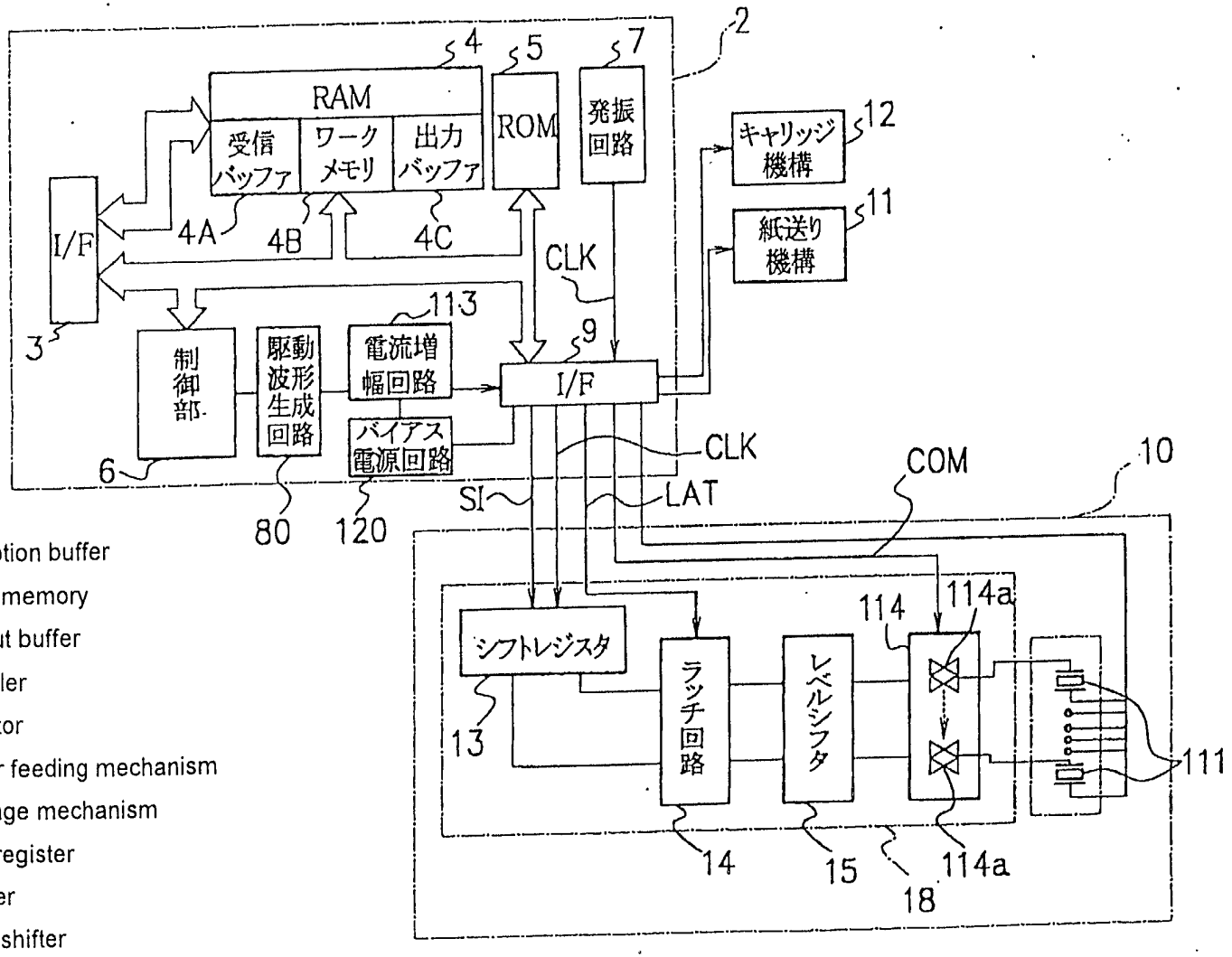
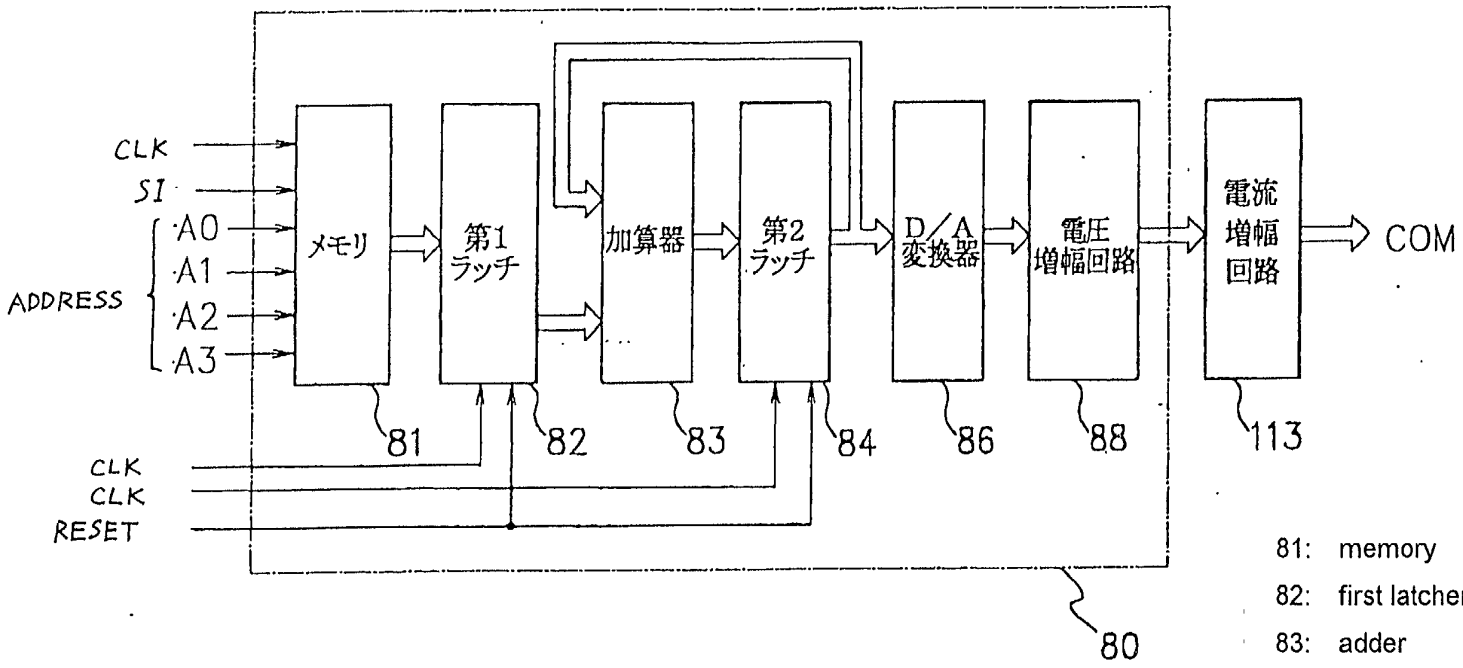
Fig. 1



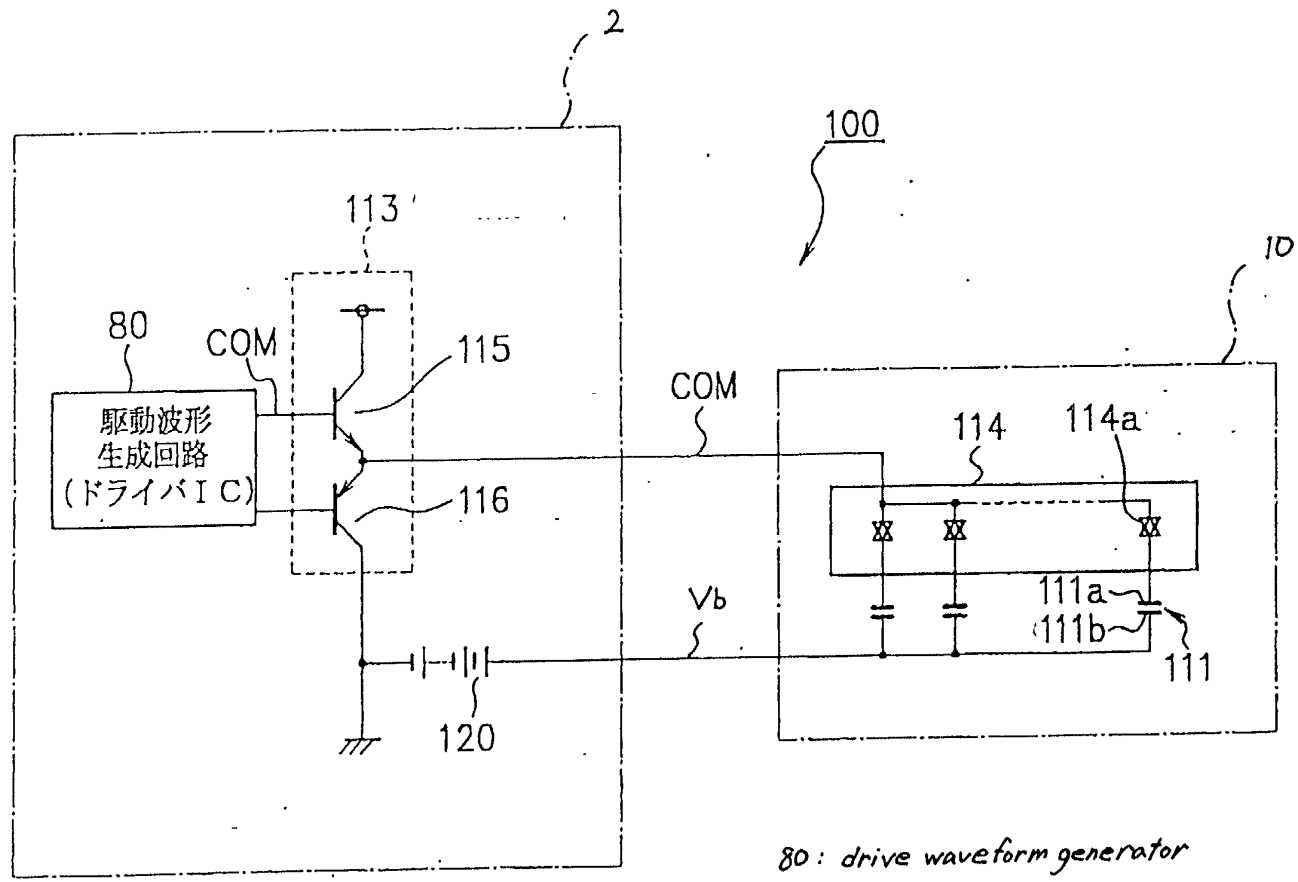
4A: reception buffer
4B: work memory
4C: output buffer
6: controller
7: oscillator
11: paper feeding mechanism
12: carriage mechanism
13: shift register
14: latcher
15: level shifter
80: drive waveform generator
113: current amplifier
120: bias power source

Fig. 2



81: memory
82: first latcher
83: adder
84: second latcher
86: D/A converter
88: voltage booster
113: current amplifier

Fig. 3



80 : drive waveform generator
(driver IC)

Fig. 4A

Fig. 4B

Fig. 4C

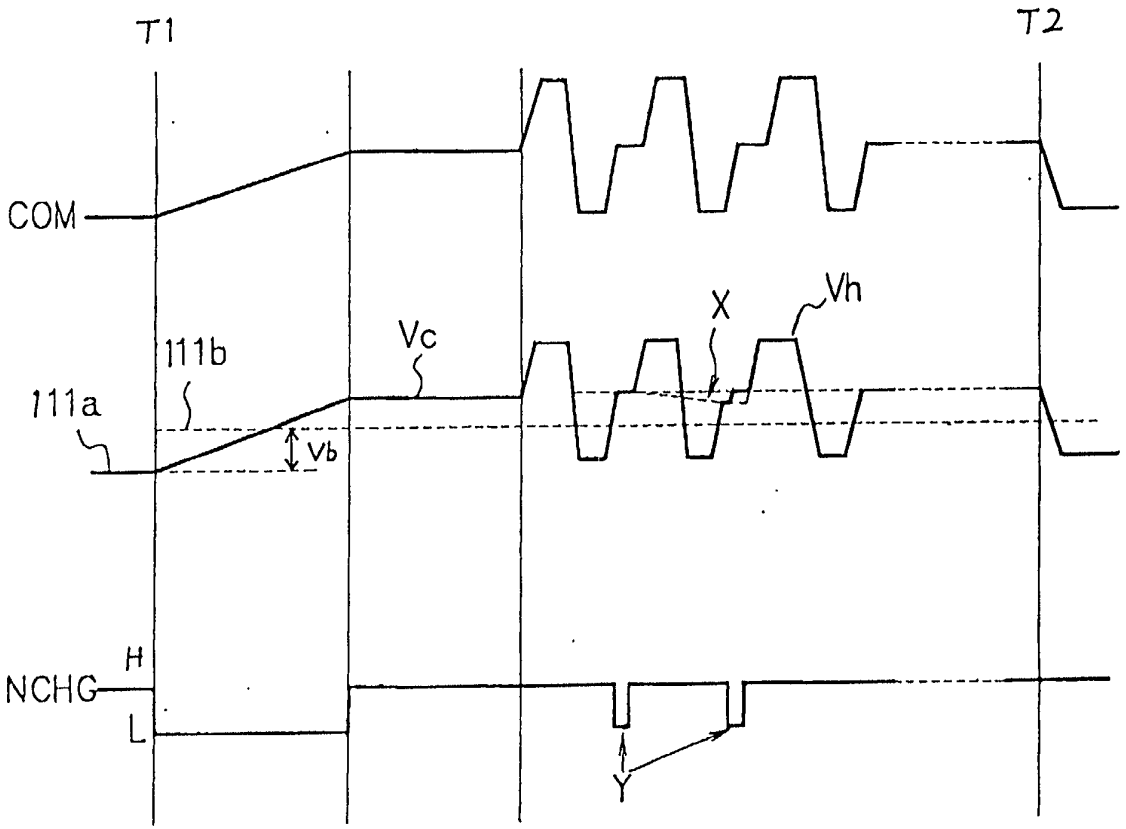


Fig. 5

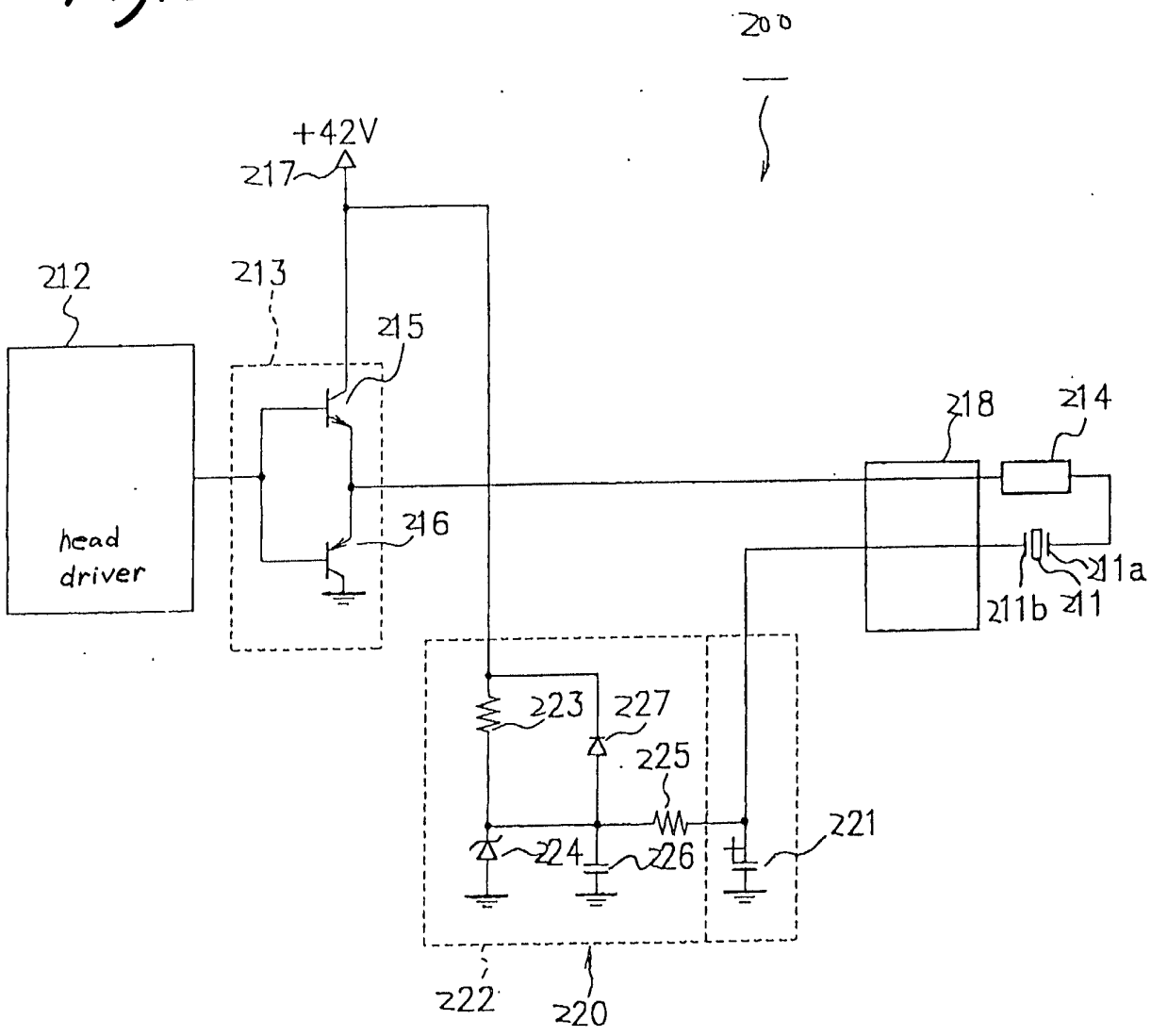

200
+42V
217
212
213
215
218
214
head driver
216
211a
211b
211
223
227
225
221
224
226
222
220

Fig. 6A

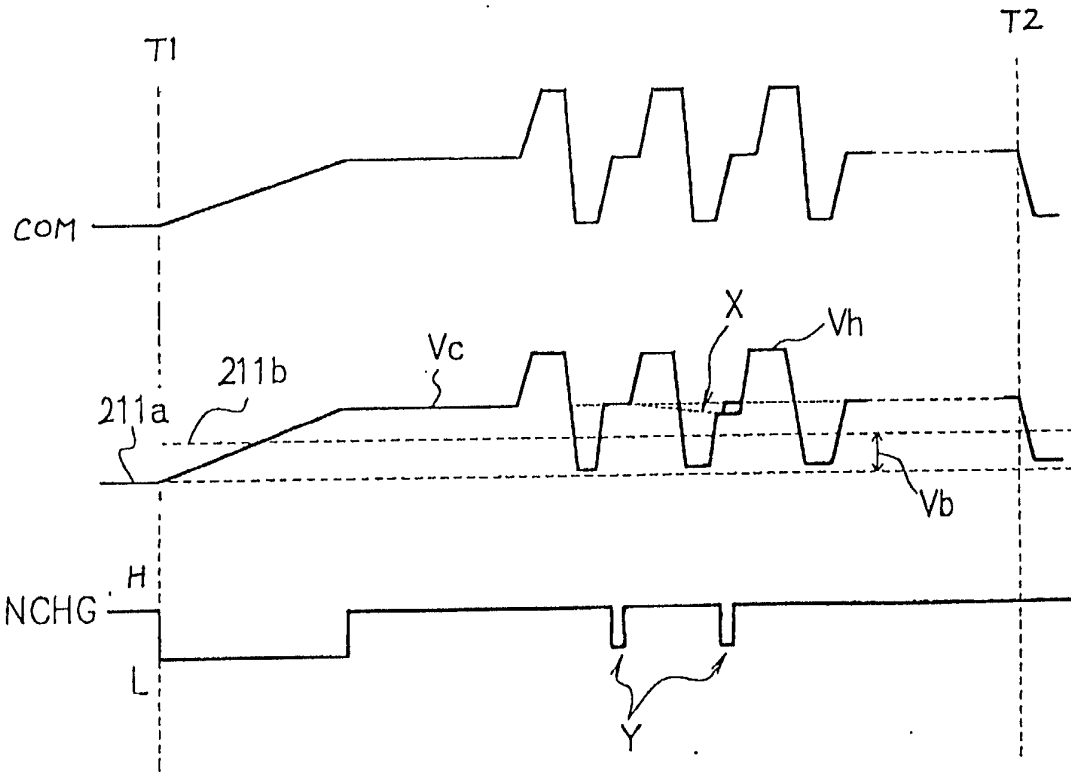


Fig. 6B

Fig. 6C

Fig. 7

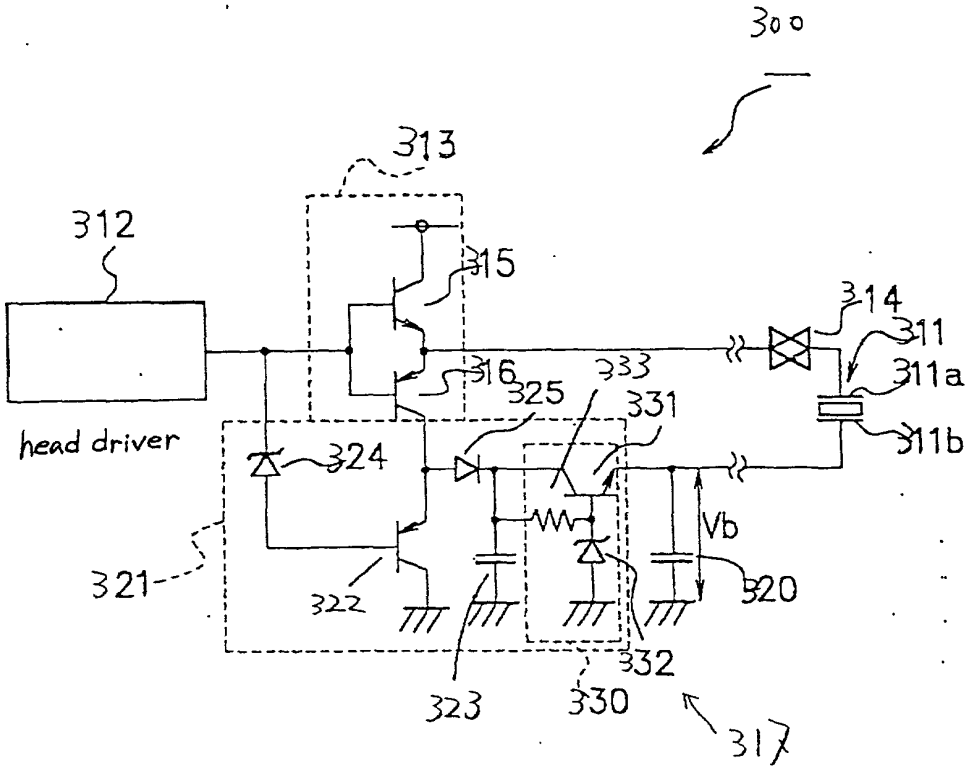


Fig. 8A

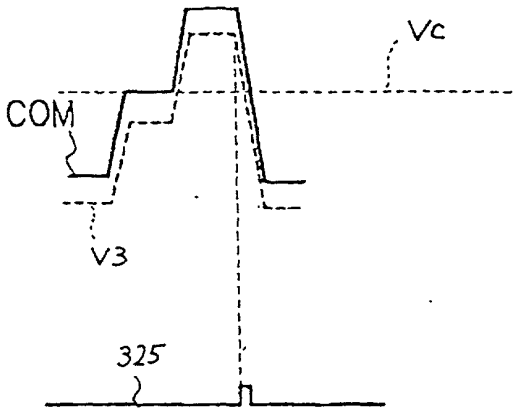


Fig. 8B

Fig. 9A

Fig. 9B

Fig. 9C

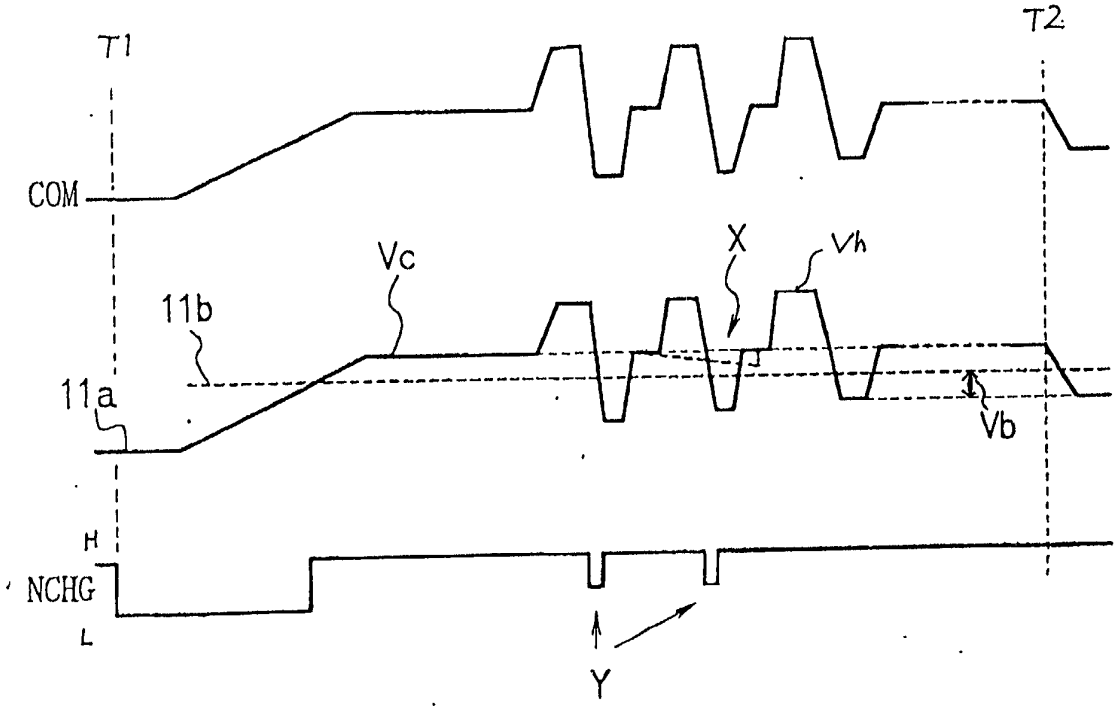


Fig. 10

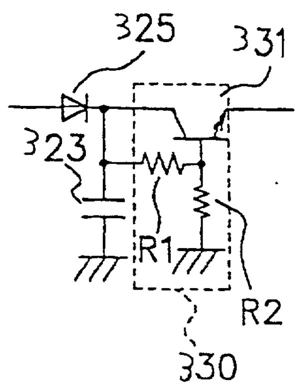

325
331
323
R1
R2
330

Fig. 11

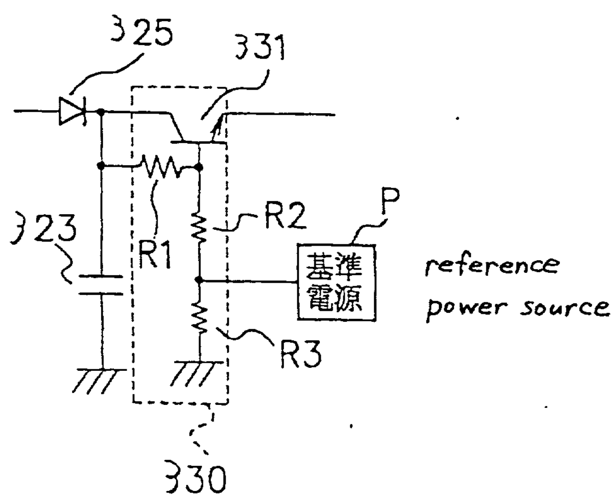

325
331
R2
P
323
R1
基準
電源
reference
power source
R3
330

Fig. 12

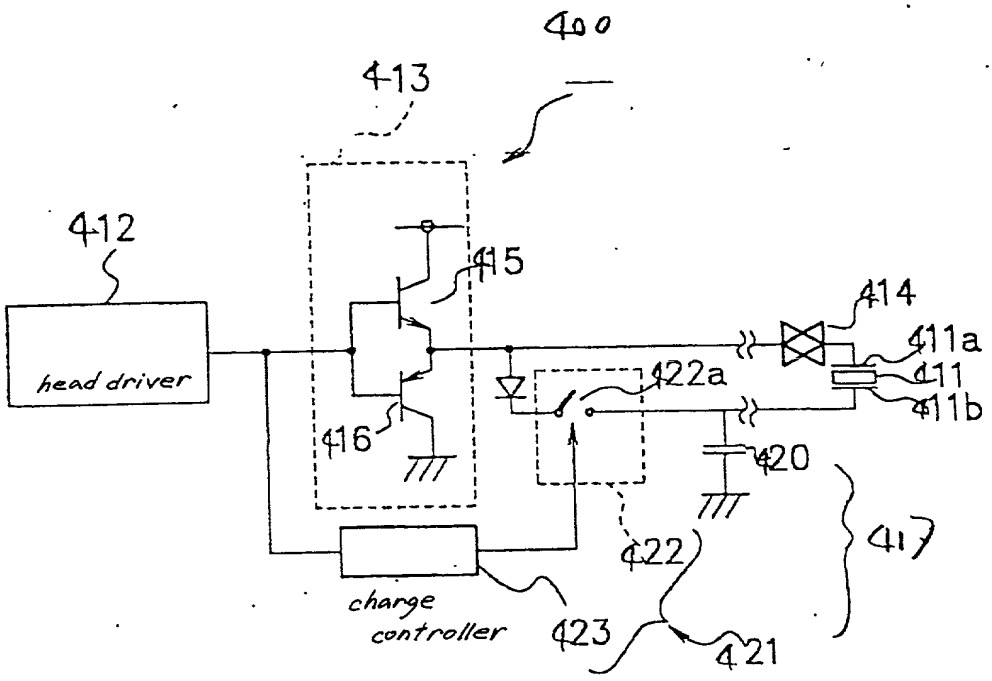


Fig. 13A

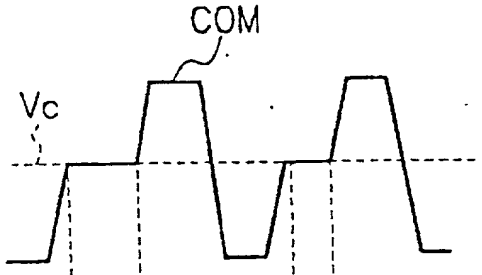


Fig. 13B

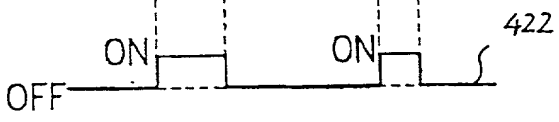


Fig. 14A

Fig. 14B

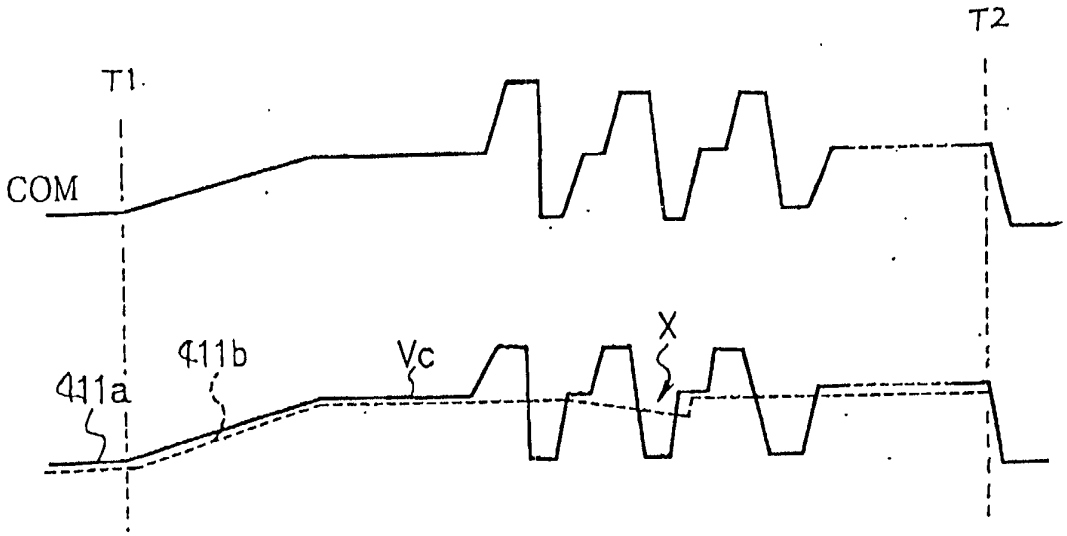


Fig. 15

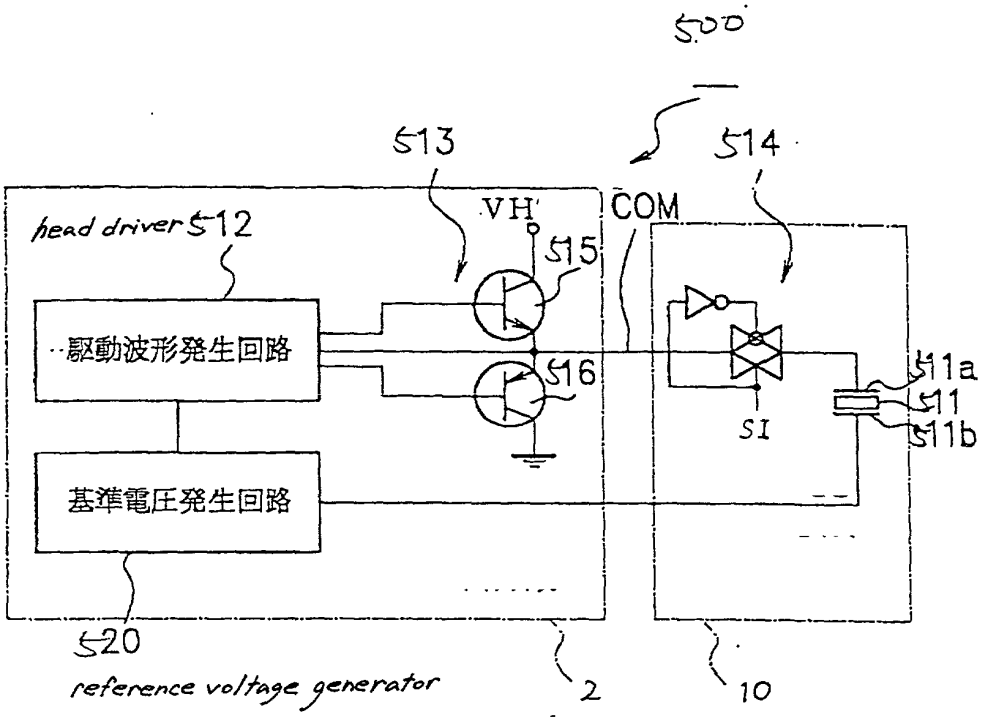

500
513
514
head driver 512
VH
COM
515
駆動波形発生回路
516
511a
511
511b
SI
基準電圧発生回路
520
reference voltage generator
2
10

Fig. 16

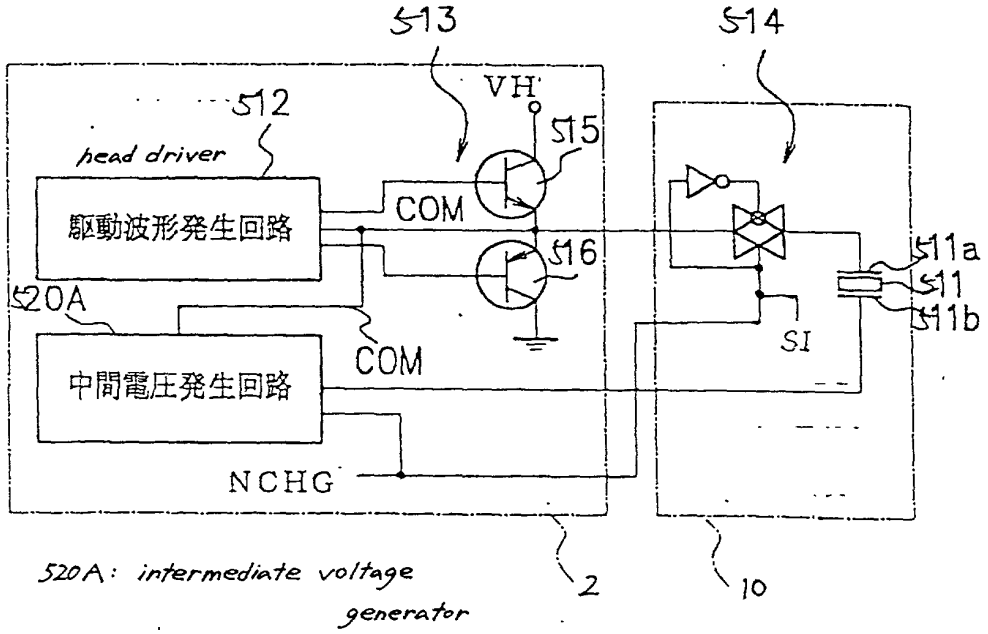

513
514
512
VH
head driver
515
駆動波形発生回路
COM
516
511a
511
511b
520A
SI
COM
中間電圧発生回路
NCHG
520A: intermediate voltage generator
2
10

Fig. 17

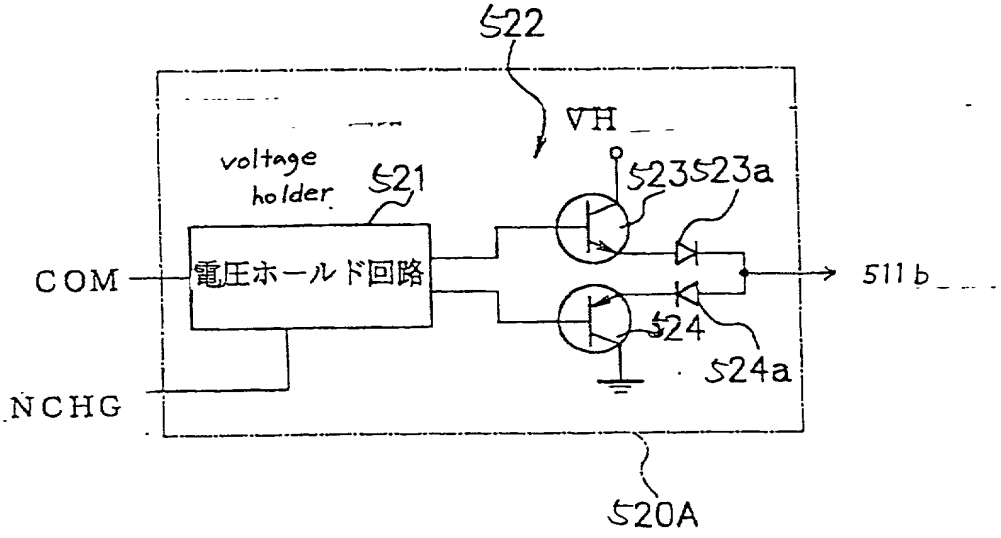

522
VH
voltage holder
521
523
523a
COM
電圧ホールド回路
511b
524
524a
NCHG
520A

Fig. 18

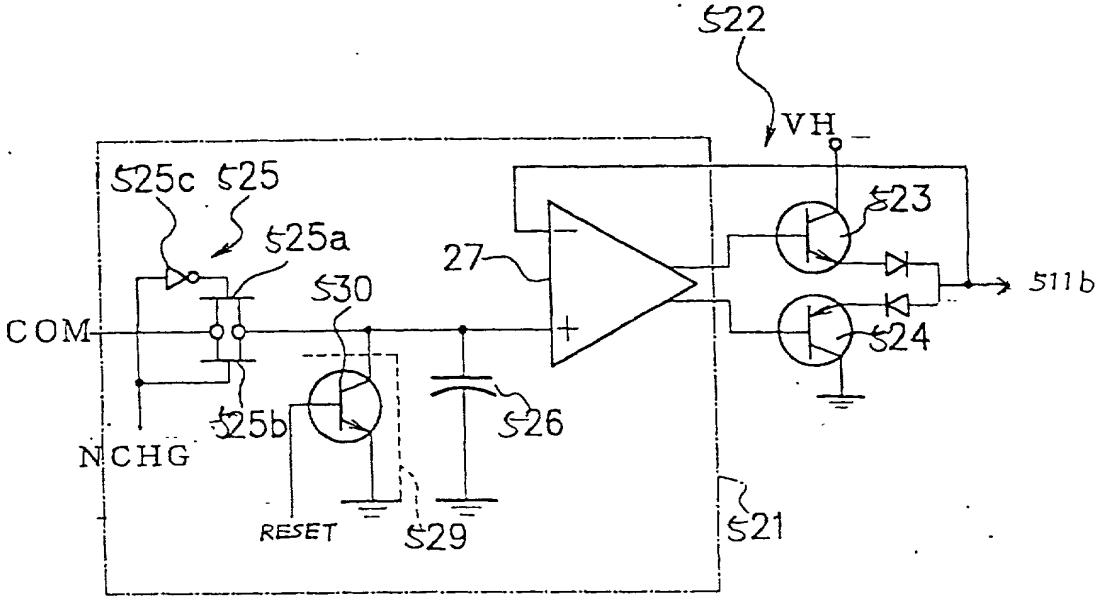

522
VH
525c
525
525a
27
523
511b
530
COM
524
525b
526
NCHG
RESET
529
521

Fig. 19A

Fig. 19B

Fig. 19C

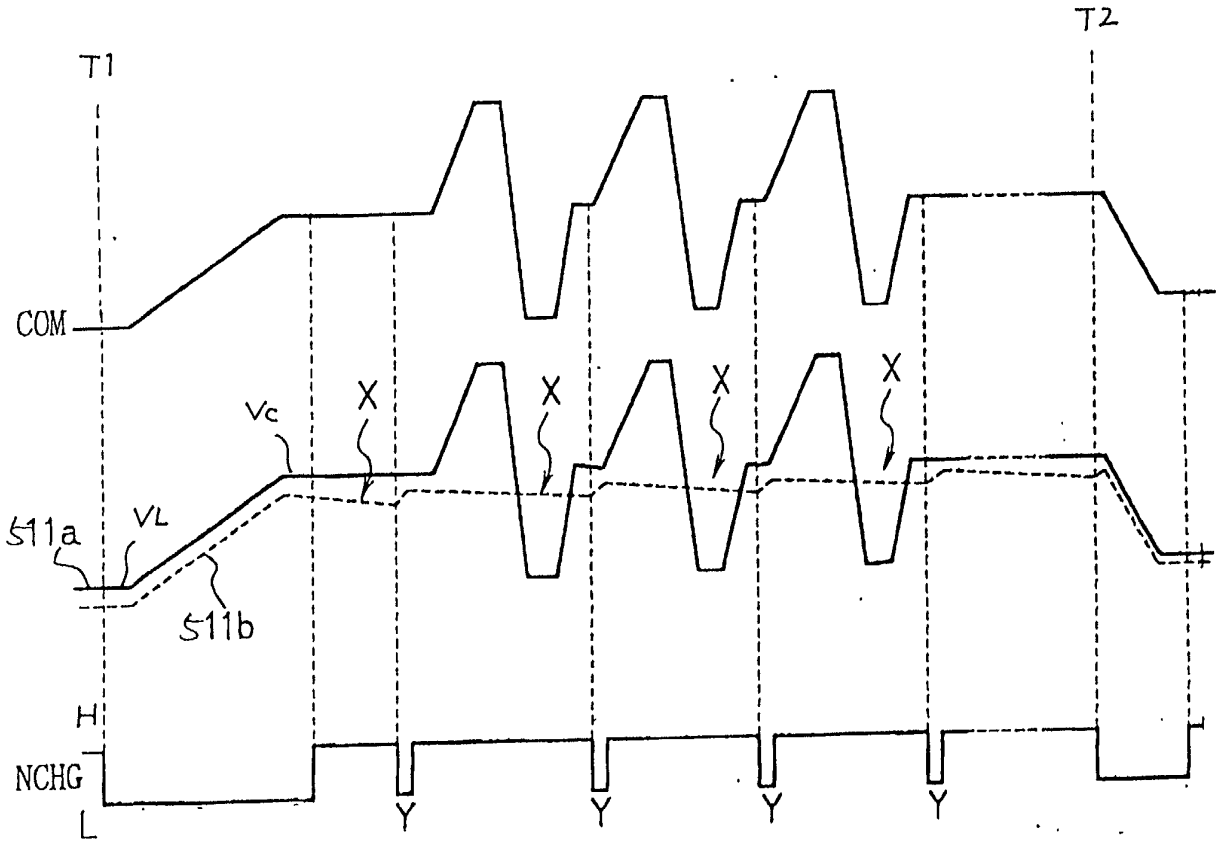
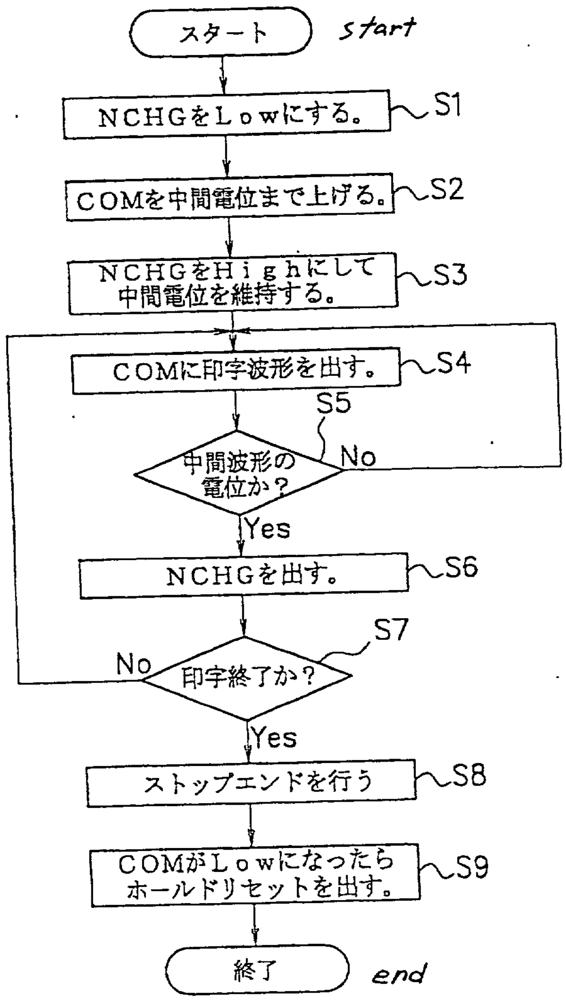


Fig. 20



S1: turn NCHG to L level

S2: boost potential of COM up to Vc

S3: turn NCHG to H level

S4: output COM to voltage holder

S5: potential of COM is lower than Vc?

S6: turn NCHG to L level

S7: printing is finished?

S8: termination processing

S9: output reset signal when potential of COM becomes VL